**Lain-Jong Li (Lance Li)**

Current position:

Professor, Chair of Future Electronics & Chair of Physics by Courtesy

Director, HKU Microelectronics center

Mechanical Engineering, University of Hong Kong

Education:

* BA (1994) and MSc (1996) of Chemistry, National Taiwan University
* D.Phil (2006) of Condensed Matter Physics, Oxford University.

Experience

* Assistant Professor, MSE, NTU (Singapore) Jun 2006 – Dec 2009
* Associate Research Fellow, Academia Sinica (Taiwan) / Feb 2010 – Apr 2014
* Research Fellow (Tenured), Academia Sinica (Taiwan) / May 2014 – Jul 2014
* Associate Professor, King Abdullah University of Science and Technology (Saudi Arabia) / Aug 2014 – Jul 2016
* Full Professor, King Abdullah University of Science and Technology (Saudi Arabia) / Aug 2016 – Dec2017
* Chief Technology Officer (CTO), Nitronix Nanotechnology,Taiwan 2015- Dec 2017
* SHARP Professor, University of New South Wales (Australia) / Sep2018-Dec 2020
* Director, Corporate Research in Taiwan Semiconductor Manufacturing Company

(Taiwan)/Dec2017-Dec2020

**Perspective on the Future Electronics Based on Two-Dimensional Materials**

Lain-Jong (Lance) Li

The University of Hong Kong

E-mail: lanceli1@hku.hk

With the dimension scaling, the transistor gate controllability becomes weaker owing to the pronounced source-drain tunneling. Hence, the transistor body thickness needs to be reduced to ensure efficient electrostatic control. New materials such as “ultra-thin” 2D semiconducting materials have attracted attention. In this talk, I would like to provide analysis and arguments on the possibility to scale the device dimension, for example down to 1nm technology node, using 2D transition metal dichalcogenides (TMD) semiconductors. At a circuit level, I shall provide our analysis on benchmarking 2D-based circuits with the state-of-the-art Si FinFETs, where we use SRAM circuits as the example to discuss the benefits of using 2D over Si FinFET (or GAA) in the technology nodes from N16 down to N1.

There are many challenges on device fabrication. Here, I we like to discuss on several major bottlenecks and the advancements we and collaborators have achieved recently. (1) We discover that hydroxide vapor phase epitaxy enables the growth of WS2 monolayers with a significantly lower density of structural defects, which make the electron mobility peaked at ~ 200 cm2/Vs. Other materials like MoS2 and WSe2 also benefit from this method (2) The mechanism of wafer-scale growth of 2D materials will be revisited. (3) Ultrahigh-k dielectrics can be applied onto short-channel (<30 nm) 2D monolayer transistors to greatly lower the subthreshold swing (down to 70 mV dec-1) with an ON/OFF current ratio up to 107. (4) Semimetal is a feasible contact metal to TMD monolayers.

